ON-CHIP LOOP FILTER FOR A PLL

ABSTRACT OF THE DISCLOSURE

An on-chip loop filter includes a 1st resistor, a 1st capacitor, a 2nd capacitor, a 3rd capacitor, a 2nd resistor, and a 4th capacitor. The 1st resistor is operably coupled to receive a charge pump output. The 1st capacitor is coupled in series with the 1st resistor where the second node of the 1st capacitor is coupled to a return. The 2nd capacitor is coupled in parallel with the series combination of the 1st resistor and 1st capacitor. The 3rd capacitor is coupled in parallel with the 2nd capacitor. The 2nd resistor is coupled to a node of the 3rd capacitor and to a node of the 4th capacitor. The other node of the 4th capacitor is coupled to ground. To enable these components to be placed on-chip, the 1st capacitor is of a 1st capacitor construct having a 1st quality factor, the 2nd capacitor is of a 2nd capacitor construct having a 2nd quality factor, where the 2nd quality factor is greater than the 1st quality factor, and the 3rd and 4th capacitors are of a 3rd capacitor construct having a 3rd quality factor, which is greater than the 2nd quality factor.